Design and Implementation of ITLC System Using FPGA

P.Giri Prasad¹, S.Vamshi Krishna²

¹(Electronics and communication Department, Godavari institute of Engineering and Technology (A), India) ²(Electronics and communication Department, Godavari institute of Engineering and Technology (A), India)

Abstract: This paper presents an idyllic method for controlling the traffic in metro cities without disturbing the surviving system. Conventional traffic systems can be installed for a non-dynamic number of intersections with fixed counts of signal durations and are typically microcontroller based. The proposed system pattern is implemented on FPGA which offers many advantages over microcontroller such fast speed, number of input/output ports and enhanced performance coupled with low than ASIC design. The system not only provides the protection but also saves the time, money and provides the polluted free environment. This paper designed of intelligent transportation of system (ITS) using VHDL. Also determines the traffic in each road by using sensors. Using the traffic status we can manage the signal time and in this way we can handle the traffic on road. On each particular way junction we can place the IR sensors which detect the traffic density and give the current traffic status particular way in the junction. Its function was verified and simulated by using Model Sim.

Keywords – ITLC, FPGA, IR Sensors, VHDL, FSM, Model Sim.

Date of Submission: 07-10-2017

Date of acceptance: 27-10-2017

I. Introduction

In recent year's implementation of smart cities are essential for sustainable urban development. One of the major problems faced by cities today is traffic congestion. Traffic light controller (TLC) is used to lessen or reduce conflicts at area shared among multiple traffic streams which is called crossings [8]. Traffic jams causes a rise in the cost of transportation as well as it affects the routine lives of people [9].

Traffic congestion is a critical difficulty in many of the cities and towns all over the world [6]. Traffic congestion has been causing many setbacks and encounters in the major and most busy cities all over the globe. To travel within the cities to the place of work or recreation has become a big problem to the commutates all along. Due to these problems people lose time, money and most importantly the energy resources will be exhausted due to the continual use in the automobiles. This traffic jam directly impacts the productivity of the workers, traders, suppliers and in all disturbing the market and raising the prices of the commodities in a way. To solve these traffic related problems, we have to build new conveniences & infrastructure but at the same time make it smart. The only drawback of making new roads on facilities is that it makes the surroundings more congested, but then this will make a way to have new ways to ease the traffic. Perhaps all the countries are working to accommodate the traffic flow and advance transportation and reduce the demand of vehicle use.

At road crossings traffic lights or traffic lamps or traffic signals are generally positioned so as to control the traffic flow. It is an electronic system generally mounted on an intersection so as to notify the safety related issues with the help of specific predefined colour system (usually red, yellow and green. Traffic light controller (TLC) has been applied using ASICs, FPGAs and microcontrollers. Some of the advantages of FPGA over microcontroller consist of the number of I/O ports, speed of processing and performance, all of which are extremely critical in the design of TLC. The cost also is an enormously important issue in design of TLC [7]. The reduced cost increasing the use of FPGAs (Field Programmable Gate Arrays) for verification and carrying out of a upcoming system.[7]

The traffic congestion due to the exploding increase of vehicles became the severest social problems and it has a major effect on the economy of a country. Therefore, many researches about traffic light system have been done in order to overcome some difficult traffic phenomenon but current research had been limited about present traffic system in well-travelled traffic scenarios. There are several models for traffic simulation. In our research we focus on optimization of traffic light controller in a city using IR sensor and Traffic light controller system by FPGA.

Many system designs that used to be built in custom silicon VLSI are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mask production of a custom VLSI especially for small quantity [1]. Through using VHDL language to the traffic light controller design, the traffic light control circuit uses digital signal automatic control to realize two groups of lights which are red, yellow and green[4] Those lights command vehicles and pedestrians passing safely at the crossroad, which bases on the data of traffic state transition [2]. There remain two kinds of the VHDL design, which are modelling and synthesis. The modelling VHDL design has major advantage in difficult design. In addition, the VHDL should not be thought as a programming language. This language is designed to describe the logic circuit. A typical model is a very helpful point to start programming the project. [3]

The FPGA traffic light control system needs to consider the present traffic situation, which is based on the data from sensors. The FPGA gets current signals of vehicles passing crossroad and base on those signals send next step order. Also, in the specific road the traffic light should be set

Specifically [1], In addition, the FPGA need to consider the time, which means splitting the traffic situation by the time [5]. In this paper we can place three sensors in each direction with some distance and we can assume first sensor give the low traffic, second sensor give the medium traffic and third give the high traffic depends sensor status we can assign the time slot in particular direction. In this paper we can implement 15 cases and develop the VHDL code these cases. But in this paper we cannot develop the hardware; we can assume the sensor position cases in four road traffic.

The rest of this paper is organized as follows: section-II reviews the literature review. In section-III, we introduce the details of the proposed scheme. Section-IV we discuss implementation details of State diagram of proposed traffic control system and Section-V present the simulation results. Finally Section-VI concludes and future scope of the paper. At the end of the paper is a list of references.

II. Literature Review

Farheena Shaikh, Dr. Prof. M. B. Chandak [2] describes an approach towards Traffic Management System using density calculation and reserve vehicle aware. In this paper, Wireless Sensor Networks organized along a road can be used to control the traffic load on roads and at traffic crossings. Sensors are deployed on either side of roads at crossing points and in reserve vehicles respectively. These sensors run on both solar energy as well as battery. Present traffic light systems have timers that are set at systematic intervals. This leads to the waste of precious time especially in case of rescue vehicles for reserve conditions. In order to control this situation, they have planned a system consisting of two parts: Smart Traffic Light Control System (STLC) and Smart Congestion Avoidance System (SCA) during emergencies. STLC System controls the change of traffic lights at crossing points giving high priority to reserve vehicles. SCA System is a smart traffic routing system that chooses the shortest routes having the smallest congestions. The system based on GPS so it has some problems in application. Thus this system is somewhat changeable.

AT&T [1] investigated with the use of useful acoustic and digital signal processing technology to produce a vehicular traffic surveillance system (Nordwall, 1994). Labeled the SmartSonic Traffic Surveillance System (SmartSonic TSS1), the plan was intended by AT&T to replace supressed magnetic loop detection systems. This technology was initially developed from research used by the U.S. Navy for submarine detection resolves. Mounted above passing vehicles, the SmartSonic [3] TSS-1 listens to the acoustic signals of vehicles and is capable of unique between larger trucks or buses and smaller vehicles. Applications to contain traffic monitoring and vehicle counting, with the potential for incident detection being an area for further research.

N. M. Z. Hashim, A. S. Jaafar, N. A. Ali, L. Salahuddin, N. R. Mohamad, M. A. Ibrahim [2] deals about Traffic Light Control System for Reserve Vehicles Using Radio Frequency. According to all these papers, a suitable wireless communication between reserve vehicles and the traffic light is by using RF. The model of this project is by the radio frequency of 434 MHz compared to the range of about 3 kHz to 300 GHz of frequency which have been reserved for the RF theoretically. After complete above researcher's clarification we can write the code for Intelligent Traffic control System in VHDL with different sensor location condition and corresponding these condition we can develop the sate diagram and these description see in section-III.

A) Compensations of FPGA over microcontroller

- FPGAs are going to rule in the coming because of their flexibility, increasingly better power efficiency and reducing prices.
- > FPGAs are flexible, you can add/ sub necessary. This cannot be done in microcontroller.
- FPGAs are favourite in military applications. There are two main reasons of that. The first object is that FPGAs are hard wired and the random attacks of the memory areas hence failure the device functionality.

- The second object is that the lifetime of FPGA based development is longer. It can be accepted for advanced chip.
- Microcontroller change too often and there is lot of rework required to do in order to keep pace technology. This is required to save the design from being obsolete.
- > The flexibility of FPGAs gives them distinct benefit over other programmable logic devices.
- FPGAs are reprogrammable and can implement any sort of logic circuits; designs can be modified after primary implementation.

III. Proposed Traffic Control System

In this proposed system, we can consider two paths i.e., (N-S) path and (E-W) path and we can place the three sensors in each direction i.e., N, S, E and W. Depending on sensors activate status we can assign the time slot. In step we can consider only one path i.e., either (N-S) path or (E-W) path. In this paper we can propose sensor status in 15 conditions and develop the VHDL code for these conditions and simulate by using Modalism. By using proposed system we reduce the traffic timing delay compare to convention traffic system. In proposed system we can consider two traffic lights i., Red and Green depends on sensor status switch ON the corresponding either Red or Green in each direction in proposed Intelligent Traffic control System.



Intelligent Traffic control System Case-1 sees in Fig.1 (a). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1 (a). The E lane has lowest level density i.e. its output is 000 i.e., 0. The W lane has lowest level density i.e. its output is 000 i.e., 0. The W lane has lowest level density i.e. its output is 000 i.e., 0. Now the data collected is 00. Now the path E gets 15 sec and path W gets 15 sec to flow in shared manner. As shown in the table-I, the E-lane traffic will first flow for 5 sec. In the directions. Then, the turn of the E-lane is stopped and the forward flow of the W-lane is started for 5 sec. Then after 5 sec, the W-lane is allowed to flow in both the directions for 5 sec. In this case the total consumed time is 15 sec and ITLCS saved 5 sec for this combination of traffic density. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-I.

Intelligent Traffic control System Case-2 sees in Fig.1 (b). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1 (b). The E lane has lowest level density i.e. its output is 000 i.e., 0. The W lane has low level density i.e. its output is 001 i.e. 1. Now the data collected is 01. Now the path E gets 15 sec and path W gets 30 sec to flow in shared manner. As

shown in the table-II, the E-lane traffic will first flow for 5 sec in both the directions. Then, the turn of the E-lane is stopped and the forward flow of the W-lane is started for 5 sec. Then after 5 sec, the W-lane is allowed to flow in both the directions for 25 sec. In this case the total consumed time is 25 sec and ITLCS saved 5 sec for this combination of traffic density. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-II.

Intelligent Traffic control System Case-3 sees in Fig.1(c). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1(c). The E lane has lowest level density i.e. its output is 000 i.e., 0. The W lane has medium level density i.e. its output is 011 i.e. 1. Now the data collected is 01. Now the path E gets 15 sec and path W gets 50 sec to flow in shared manner. As shown in the table-III, the E-lane traffic will first flow for 5 sec. Then after 5 sec, the W-lane is allowed to flow in both the directions for 35 sec. In this case the total consumed time is 45 sec and ITLCS saved 5 sec for this combination of traffic density. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-III.

Intelligent Traffic control System Case-4 sees in Fig.1 (d). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1 (d). The E lane has lowest level density i.e. its output is 000 i.e., 0. The W lane has high level density i.e. its output is 111 i.e. 1. Now the data collected is 01. Now the path E gets 15 sec and path W gets 70 sec to flow in shared manner. As shown in the table-IV, the E-lane traffic will first flow for 5 sec in both the directions. Then, the turn of the E-lane is stopped and the forward flow of the W-lane is started for 5 sec. Then after 5 sec, the W-lane is allowed to flow in both the directions for 55 sec. In this case the total consumed time is 65 sec and ITLCS saved 5 sec for this combination of traffic density. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-IV.

Intelligent Traffic control System Case-5 sees in Fig.1 (e). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1 (e). The E lane has low level density i.e. its output is 001 i.e., 1. The W lane has lowest level density i.e. its output is 000 i.e. 0. Now the data collected is 10. Now the path W gets 15 sec and path E gets 30 sec to flow in shared manner. As shown in the table-V, the W-lane traffic will first flow for 5 sec in both the directions. Then, the turn of the W-lane is stopped and the forward flow of the E-lane is started for 5 sec. Then after 5 sec, the E-lane is allowed to flow in both the directions for 25 sec. In this case the total consumed time is 25 sec and ITLCS saved 5 sec for this combination of traffic density. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-V.

Intelligent Traffic control System Case-6 sees in Fig.1 (f). In this figure we consider (E-W) path see red lines in figure. Now when the timings of the N-S stops then the sensor data collected is as shown in the Fig.1 (f). The E lane has medium level density i.e. its output is 001 i.e., 1. The W lane has medium level density i.e. its output is 001 i.e. 0. Now the data collected is 11. Now the path W gets 30 sec and path E gets 30 sec to flow in shared manner. As shown in the table-VI, the W-lane traffic will first flow for 10 sec in both the directions. Then, the turn of the W-lane is stopped and the forward flow of the E-lane is started for 10 sec. Then after 10 sec, the E-lane is allowed to flow in both the directions for 10 sec. In this case the total consumed time is 30 sec. Same way apply in N-S direction in this case we can E-W direction sensors stopped then collect the sensor status in N_S direction and give the time see Table-VI. Hence ITLCS saved 5 sec for this combination of traffic density. Similarly time has been saved in all other combinations of traffic density. In this paper we consider 16 cases, if we explain these cases then we can utilize more papers that's why in this paper we can design FSM modeling of proposed traffic control system and also design flow chart. This flow chart apply in each case final this cases developed in VHDL and simulate by using Model Sim. Table-I, II, III, IV, V and VI: Intelligent Traffic control System Sensor Status and corresponding traffic light timing





IV. FSM Modeling of Proposed Traffic Control System

The state diagram of proposed traffic control system sees in Fig.2. In this figure we can consider 15 states and each state we consider two paths i.e., (N-S) and (E-W) path and control operation done each time only consider one path. In this diagram we can use NS (North Sensors),SS (South Sensors),ES(East Sensors) and (West Sensors) and each pole we can place three sensor. In this, first sensor indicate the low traffic density and assign 25 sec for ON time for Green light for that direction this same utilize for clear the traffic for remaining direction, second sensor indicate the medium traffic density and assign 35 sec for ON time for Green light for that direction this same utilize for clear the high traffic density and assign 55 sec for ON time for Green light for that direction this same utilize for clear the traffic for remaining direction. In this paper develop the VHDL code ON indicates binary '1' and OFF indicates binary '0'.



The simulation code done in above diagram in this diagram decision box contains E-W path and N-S path depends on condition we can consider corresponding outputs. In this we can consider 16 outputs and this outputs ON depends on sensor status.

V. Simulation Results

The synthesis is performed by Xilinx 7.1. The RTL Schematic of proposed system see in Fig.5 and Technology Schematic see in Fig.4.



Fig.4 RTL Schematic of Proposed Traffic control system

The VHDL test bench for all possible cases was simulated by using the ModelSim by Xilinx 7.1 and the results offered complete success is shown in Fig.5



. Fig.5 Simulation results of test_bench program of Proposed Traffic control system

VI. Conclusion and Future Scope

As with the increasing population, the traffic is also increasing in proportion. Hence we required a powerful system which can effectively control the increasing traffic problem. Therefore proposed Traffic Control System contributes to a great extent in solving the traffic problem. It can save a lot of time of people, which is presently being wasted due to the current traffic system. If the traffic is controlled effectively, it can even help in reducing the heavy pollution that vehicles donate to the environment. Having an effective traffic control system, probability of accidents can be reduced to a greater extent. The proposed traffic control system implemented in VHDL Code also simulation done by using ModelSim.

In case, if there is any kind of problem occurs in the traffic system, it also has an option of manual control i.e. when the system becomes faulty then the whole system can be manually operated, which again adds to its advantages.

Another prospect of it is that, the installation cost of this system will not be more as compared to the already existing system. Hence, this system is cost effective.

Therefore, proposed Traffic Control System has a bright future ahead and it can help in solving the traffic problem of the already existing system.

After observing the whole system, we conclude that in order to deal with the present traffic problem, proposed Traffic Control System is required to be installed. It is better than the present traffic system in many ways like it saves a lot of time by dividing the time for every path by observing the traffic density of the respective path. It helps in reducing the pollution problem by to a greater extent by allowing a proper flow of traffic.

It also helps in reducing the accident chances by dividing the sufficient time slot to any path by observing the traffic density of the path; hence any user won't be any hurry to give rise to any accidental incidents.

References

- S. Nath "Design Design of a FPGA based Intelligent Traffic Light Controller with VHDL", Radar Communication and [1] Computing (ICRCC) 2012 International conference pp- 92-97
- [2]
- Traffic light, wikipedia, the free encyclopedia Available: <u>http://en.wikipedia.org/wiki/traffic light</u> Jose E. Ortiz and Robert H. Klenke "Simple Traffic Light controller : A digital system design project", IEEE Southeast [3] conference 2010 (Southeast conference), Concord, NC, March 2010, pp 85-88
- L. Zhenggang, X. Jiaolong, Z. Mingyun and D. Hongweis "FPGA based Dual mode Traffic Light System Design", Information [4] Science and Engineering (ICISE) 2009 First International Conference, Dec. 2009, pp. 558-561.
- W.M. El- Medany "FPGA based Advanced Real Traffic light controller system design", Technology and Applications 2007. [5] IDAACS 2007, 4th IEEE workshop, pp. 100.
- http://seminaprojects.org/t-traffic-signal-controller [6]
- "FPGA-Based Advanced Real Traffic Light Controller System Design". El-Medany, W.M. ; Univ. of Bahrain, Sakhir ; Hussain, [7] M.R.DOI:10.1109/IDAACS.2007.4488383 Publisher:IEEE
- [8] Sabri, M.F.M.; Husin, M.H.; Abidin, W.A.W.Z.; Tay, K.M.; and Basri, H.M., "Design of FPGA-based Traffic Light Controller System," in Computer Science and Automation Engineering (CSAE), 2011 IEEE International Conference on , vol.4, no., pp.114-118, 10-12 June 2011
- [9] Jaap Vreeswijk; and Robbin Blokpoel, "Fuel and emission Factors-How much can We realistically reduce with ITS?" 9th ITS European congress, Dublin Ireland, 4-7 June 2013

IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) is UGC approved Journal with Sl. No. 5016, Journal no. 49082.

P.Giri Prasad. "Design and Implementation of ITLC System Using FPGA." IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), vol. 12, no. 5, 2017, pp. 07–13. _____I

.